Novel Active Differential Phase Splitters in RFIC for Wireless Applications

Huainan Ma, *Member, IEEE*, Sher Jiun Fang, Fujiang Lin, *Member, IEEE*, and Hiroshi Nakamura

***Abstract*— Two novel active differential phase splitters have been designed and fabricated in a GaAs MESFET process. The new circuits employ a concept of feedback to adjust gain and phase unbalance separately and accurately. The active phase splitters feature simplicity, low power supply, and wide-band performance. The circuits can provide ±1 dB and 180 ± 1° differential signals within 4-GHz bandwidth, well covering the frequency range currently used for dual-band commercial wireless communications. In narrow-band application, more accurate balanced differential signals can be achieved by external tuning.**

***Index Terms*—Baluns, differential amplifiers, MMIC's, MMIC phase shifters, phase shifters.**

I. Introduction

DIFFERENTIAL phase splitters (or baluns) are basic cells required in microwave components such as balanced mixers, multipliers, and phase shifters. An ideal differential phase splitter will generate a pair of differential signals which have balanced amplitude and phase (0 dB gain difference and 180° phase difference) from a single input.

In RFIC there are passive and active differential phase splitters or baluns. *LC* networks can be used for narrow-band passive baluns; microstriplines can be used for wide-band passive baluns [1]. However, the spiral inductors, MIM capacitors, and microstriplines in RFIC are too expensive due to their larger physical size at lower microwave frequencies. There are three categories of active balun circuits normally employed in lower microwave frequencies for wireless communications: single FET circuits [2], [3], common-gate common-source circuits [4], [5], and differential amplifier circuits [6], [7].

The single FET active circuit is only useful at low frequencies. At higher frequency range, the circuit is limited by the imbalances caused by the parasitic capacitance of the FET. The best result obtained from this type of structure is 1 dB and 176° at 950 MHz [3]. To make it applicable at higher frequency, a sophisticated imbalance cancellation technique was used to improve the performance beyond 1 GHz [2]. It had 1 dB amplitude difference and 172° phase difference (−8° unbalance) from 700 MHz to 1.7 GHz. However, the tradeoff was the increase of circuit complexity, die area, and dc current. For accurate results beyond 2 GHz, the application of the single FET circuit is questionable.

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H. Ma was with the Institute of Microelectronics (IME), Singapore, Science Park II, Singapore 117685, Singapore. He is now with the Wireless IC Design Center, Fujitsu Microelectronics, Dallas, TX 75252-5675 USA.

S. J. Fang, and F. Lin are with the Institute of Microelectronics (IME), Singapore, Science Park II, Singapore 117685, Singapore.

H. Nakamura is with the Oki Techno Centre (Singapore) Pte. Ltd., Singapore 117674, Singapore.

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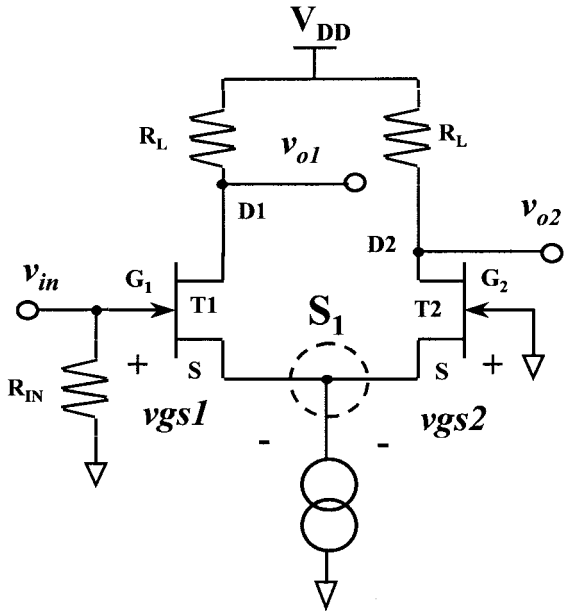
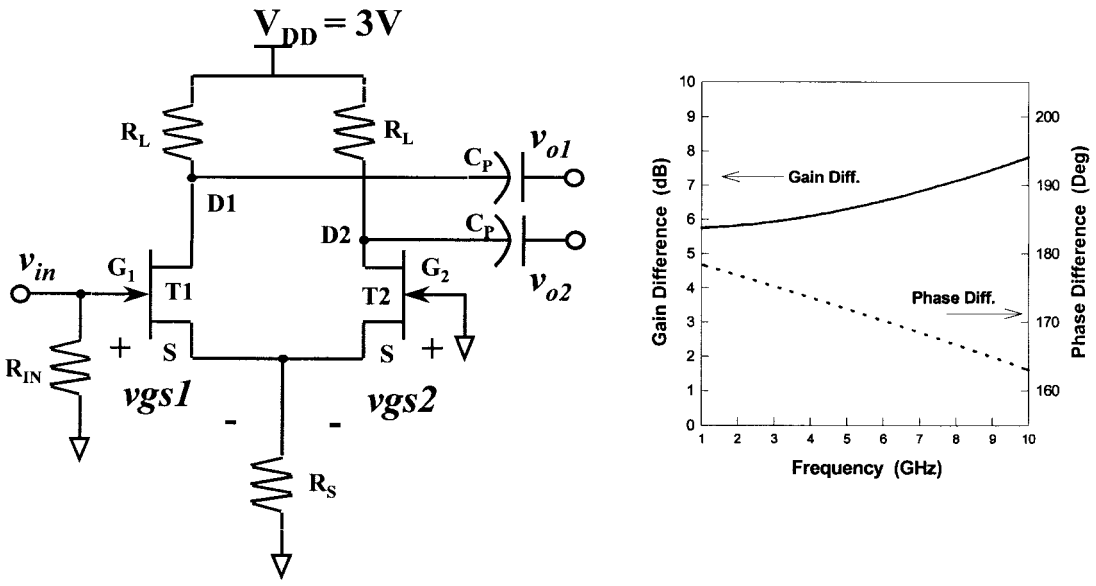


Fig. 1. Differential amplifier as phase splitter.

The common-gate common-source (CGCS) circuit provides equal amplitudes split with 180° phase difference [4], [5]. In this configuration, the ac coupling capacitance and bypass capacitance need to be adjusted separately to optimize at a specific frequency to achieve balanced differential signals. Therefore, this configuration is only good for narrow-band applications. The gain and phase differences at 1.67 GHz from this configuration are around 0.5–2 dB and 177–189° due to the process variation and asymmetric signal path.

The differential amplifier circuit is shown in Fig. 1. Ideally, this circuit will provide equal amplitude (or gain) and 180° phase difference. However, due to the finite impedance at node S1 caused by strong parasitic at high frequency, the gain and phase balance are poor.

An active device is often used as the current source. However, besides the finite impedance at node S1, the voltage drop across the drain and source make it difficult to realize in low power supply circuit as required by the portable wireless applications ($V_{DD} < 3$ V or even < 2 V). Our simulation showed that in this configuration, the output amplitude difference can be 2 dB or the phase difference can be poorer than 174°, within frequency range from dc to 6 GHz.



(a) (b)

Fig. 2. (a) Circuit diagram of the simple differential pair with a biasing resistor R_S and (b) simulated gain and phase differences versus frequency for circuit (a).

In [6], the active current source was replaced by an inductor to increase the impedance of S1 at high frequencies. When an ideal inductor with unlimited value (dc through and ac block) is used as the current source, excellent results can be obtained. However, this extra large ideal inductor is not viable to be realized on-chip. An 8.6-nH on-chip spiral inductor that occupied the die area of 250 $\times$ 250 μm^2 is used in our simulation. This circuit obtained 1 dB gain difference and 175° phase difference at 7.5 GHz, at other frequencies, the gain and phase balance are poor. Therefore, it is only applicable for narrow-band applications. Bigger spiral inductors which have lower self-resonant frequencies can be used for phase splitters with lower application frequency but they occupy even more die area. Therefore, this topology is not suitable for RF communication applications where the frequencies are now generally below 2 GHz.

In many cases, a biasing resistor R_S is used instead as shown in Fig. 2(a). For the differential amplifier pair, the input ac signal $v_{\rm in}$ will be divided into two parts, v_{gs1} across gate and source of T1 and v_{gs2} across source and gate of T2. Suppose T1 and T2 have the same common source input impedance z, and then v_{gs1} and v_{gs2} have the following relation:

$$v_{\rm in} = v_{gs1} - v_{gs2} - \frac{v_{gs2}}{v_{gs1}} = \frac{R_s//z}{z} = \frac{R_s}{R_s + z}. \quad (1)$$

Equation (1) shows that when $R_S \to \infty$, $v_{gs1} = -v_{gs2} = v_{in}/2$, the output signals must be balanced, and this is the low frequency case with an ideal current source at the bottom. When $R_S \to 0$, $-v_{gs2}/v_{gs1} = 0$, which means $v_{gs2} = 0$ and $v_{gs1} = v_{\rm in}$, no input signal reaches T2 at all. In the general case, $|v_{gs1}| > |v_{gs2}|$ and their phase difference is not 180°, therefore their output signals are not balanced, see Fig. 2(b). To overcome this problem, a compensation method was invented [7], where complicated compensation circuits make the balun design more difficult and some compensation circuits consume more power.

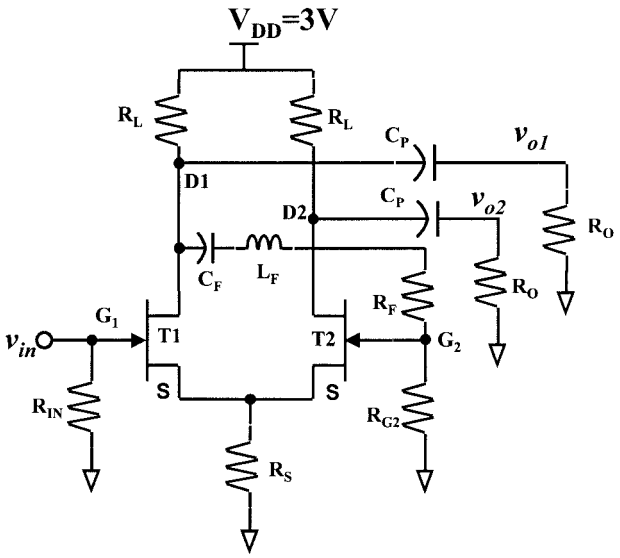


Fig. 3. Circuit 1, the differential phase splitter with a series *LCR* feedback balancing circuit.

In contrast to the approaches mention above, this paper proposes two novel circuits [8]. Section II describes the proposed novel phase splitter circuits, Section III presents the simulation and measurement results, and Section IV gives conclusions.

II. Circuit Description

The two novel active differential phase splitters proposed here use a concept of *LCR* feedback to adjust gain and phase unbalance separately and accurately. In the feedback circuit, a tunable resistor can be realized by using a MESFET to tune the unbalance caused by the process variations. The circuits were realized successfully by using a 0.5-μm depletion MESFET

TABLE I
SIMULATED GAIN AND PHASE DIFFERENCES AGAINST PROCESS VARIATIONS

Circuit 1		Optimized@1.67GHz		Optimized@5.8GHz	
Variation Items	Mismatch Values	ΔGain (dB)	ΔPhase (Deg)	ΔGain (dB)	ΔPhase (Deg)
ΔV_P	± 20mV	− 0.15 ~ 0.11	179.5 ~ 179.6	− 0.16 ~ 0.16	180.0 ~ 180.1
ΔC_F	± 20%	− 0.026 ~ − 0.027	179.7 ~ 179.4	− 0.0045~ − 0.0037	180.2 ~ 179.9
ΔC_P	± 10%	− 0.027~ − 0.026	179.7 ~ 179.4	0.0011~ − 0.032	178.9 ~ 180.2
ΔR_L	± 10%	0.17 ~ − 0.26	179.2 ~ 179.9	0.21 ~ − 0.16	179.2 ~ 180.9
$\Delta (R_F / R_{G2})$	± 10%	0.17 ~ − 0.26	179.2 ~ 179.9	0.34 ~ − 0.39	179.5 ~ 180.6

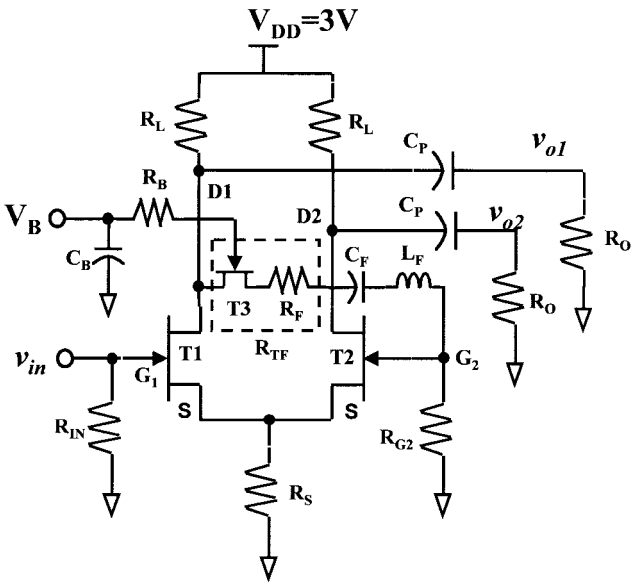


Fig. 4. Circuit 2, the tunable active differential phase splitter.

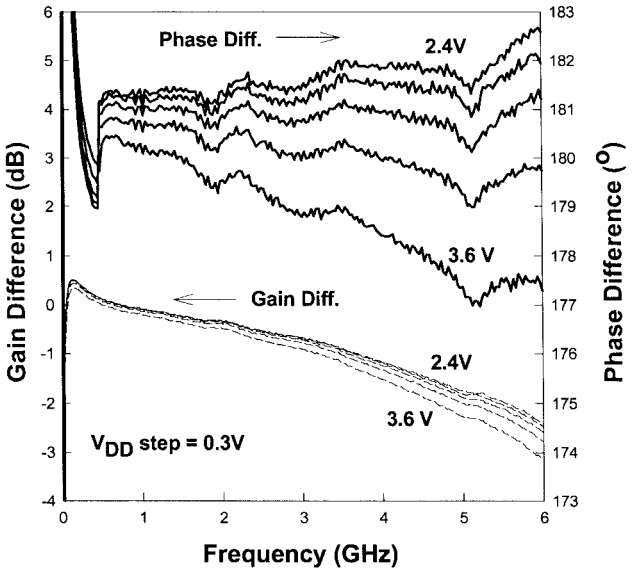


Fig. 6. Measured gain and phase differences versus frequency with variation of V_{DD} for circuit 1.

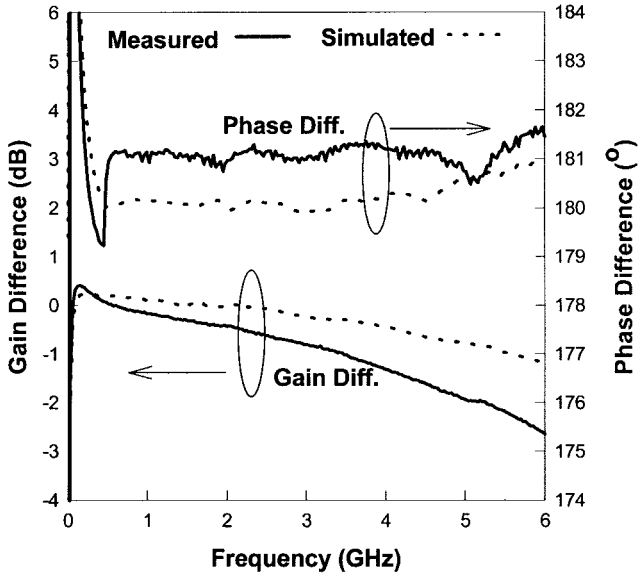


Fig. 5. S-parameter dataset simulated results versus measured results for circuit 1.

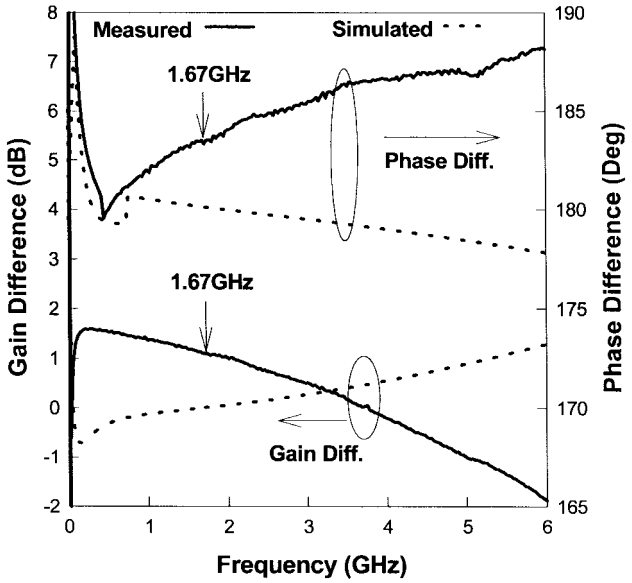
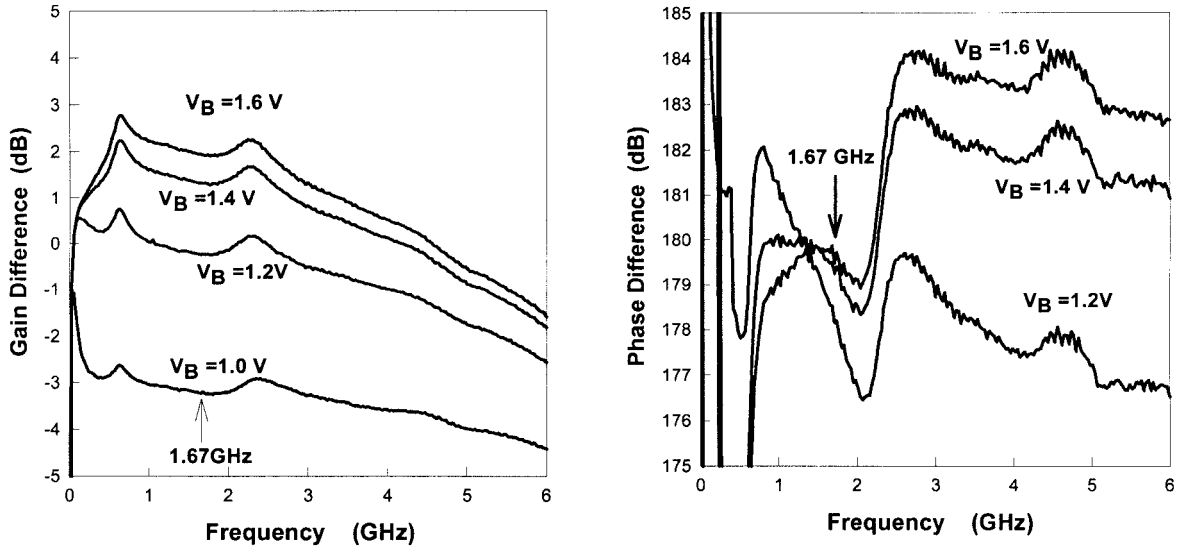


Fig. 7. EEFET3 simulation results versus measured results for circuit 1.

technology with pinch-off voltage $V_P = -0.9$ V. Both circuits are shown in Figs. 3 and 4, respectively.

A. Circuit 1

Examining Fig. 2(a) and (b), it is seen that the amplitude of v_{O1} is bigger than that of v_{O2} by 6–8 dB. The phase difference ranges from 180° at the lower end of frequency range to 163° at the higher end of frequency range. Since Fig. 2(a) has a symmetrical configuration of R_L, C_P, and R_O, the unbalanced v_{O1} and v_{O2} are due to the unbalanced input signals to T1 and T2 as mentioned in (1). To balance the output power at v_{O1} and v_{O2}, the input power v_{G2} at node G2 needs to be increased.



(a) (b)

Fig. 8. (a) Measured gain differences versus frequency and (b) measured phase differences versus frequency with external tuning of V_B in circuit 2.

This requirement can be realized by feeding a certain amount of the signal power from D1 to G2.

Based on this idea, a series *LCR* feedback circuit, connecting D1 through G2 to ac ground, is proposed as shown in Fig. 3. The feedback circuit consists of two resistors R_{G2} and R_F, an inductor L_F, and a capacitor C_F. This feedback circuit will help to reduce the v_{O1} power and increase the v_{O2} power. The resistor R_{G2} plays two roles: it keeps dc bias of T2 the same as T1, at the same time it senses the signal fed back from D1. C_F provides a dc blocking function so that the feedback circuit will not shift dc bias of T2. At the application specific frequency ω, if C_F and L_F values are chosen in such a way that they follow the equation of

$$L_F \bullet C_F = \frac{1}{\omega^2} \tag{2}$$

the phase delay from D1 to G2 is zero. This is because that the series *LC* circuit gives a zero reactance at its resonant frequency. When this happens, the feedback *AC* equivalent circuit will reduce to R_F, R_{G2}, and z_2, where z_2 is T2's gate input impedance at ω. AC signals v_{G2} and v_{D1} have the following relationship:

$$v_{G2} = v_{D1} \bullet \frac{R_{G2}//z_2}{R_F + R_{G2}//z_2}. \tag{3}$$

From (3), v_{G2} can be changed by adjusting R_F and R_{G2}.

The amplitude tuning of the phase splitter will be taken care of by the ratio of R_F and R_{G2}. The phase unbalance can be adjusted by proper choice of reactance of the feedback circuit. The reactance X_F is given as

$$X_F = \omega L_F - \frac{1}{\omega C_F}. \tag{4}$$

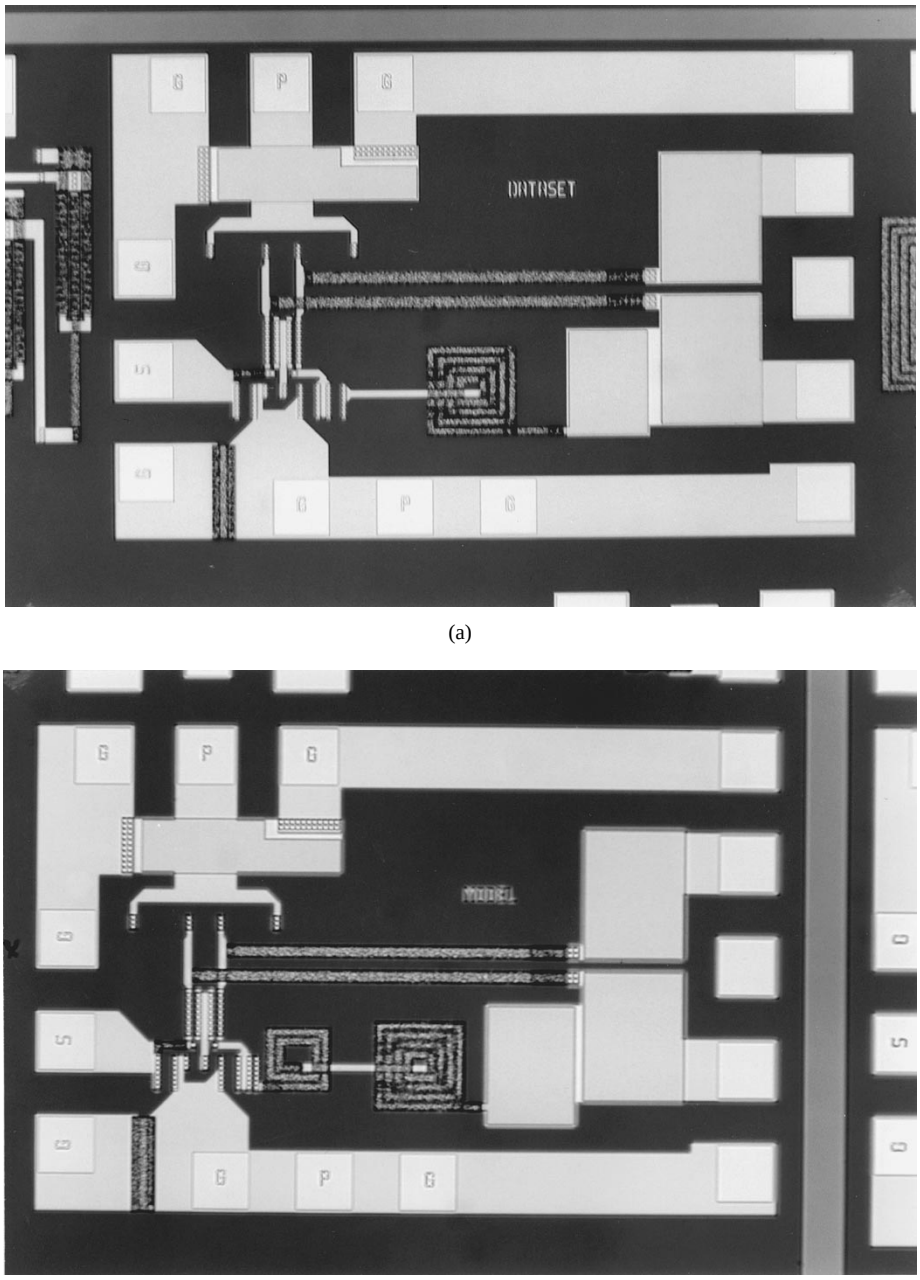
X_F can be positive (inductive), zero (resistive), or negative (capacitive) by adjusting L_F and C_F values at the application frequency Ω. Thus, the phase unbalance at output ports can be effectively cancelled. From (4), it is seen that the phase tuning can be done in a linear mode by changing L_F and keeping C_F constant since $X_F \propto L_F$, or in nonlinear mode by changing C_F and keeping L_F constant, or by changing both. The Q factor is not important in this design because the lossy part of the inductor can be treated as part of R_F in the feedback circuit. In RFIC design, the actual choice of L_F and C_F depends on the consideration of area consumption, phase tuning sensitivity, and process tolerances.

It is clear that the output termination impedance R_O will affect the choice of values of the components in the feedback circuit. When R_O is zero, v_{D1} is coupled to ground through C_P. When R_O is open (taken away), v_{D1} goes through the feedback circuit completely.

B. Circuit 2

To achieve even more accurate results in certain high-performance RF applications, the unbalance caused by the element variations in the previous circuit should be cancelled. The element value variations come from manufacturing tolerances, temperature variations, aging, etc. The solution to this could be adding some tuning circuits to the phase shifter to adjust any variation caused by the changes of element value. The second circuit, which is based on the first one but externally tunable, is shown in Fig. 4.

In this new circuit, an extra MESFET T3 is connected in series with the feedback resistor R_F. The externally changeable dc voltage V_B will adjust the channel resistance of T3. Thus T3 and R_F are considered as a combined variable feedback resistor R_{TF}. T3 and R_F are relocated to node D1. This relocation keeps V_B operating in a positive range ($0 < V_B < V_{DD}$) for the depletion MESFET which has the negative pinch-off voltage. In the circuit design, the initial bias point of V_B, the size of T3, and the values of R_F and R_{G2} are chosen in such a way that external tuning of V_B will vary the gain and the phase balance within a specific small range centered at the balanced point. In this way, the unbalance (or offset of gain) of the differential signals caused by the process



(a)

(b)

Fig. 9. Chip microphotographs of: (a) circuit 1 and (b) circuit 2.

variations can be effectively cancelled in high-performance RF applications.

III. Simulation and Measurement

Both circuits were designed and optimized at 1.67 GHz for the PHS application and the results were verified through on-wafer S-parameter measurement. The transistor models used in the simulation are based on: 1) dataset—measured S-parameters at fixed biasing point, and 2) extracted HP EEFET3 model.

Fig. 5 is the simulation using S-parameter dataset against the measurement results of circuit 1. The gain difference of ± 1 dB and phase difference of $180 \pm 1^{\circ}$ have been easily achieved within 0.5–3.5 GHz frequency range. It covers all frequencies currently used for commercial wireless communication systems. If the circuit was optimized for wider-band applications, the same results could be obtained within 4 GHz bandwidth. Since the circuit is based on the symmetrical differential pair and has a broadband performance, this feature makes it have the best performance against IC process variations. Table I is the simulation of gain and phase difference against variation or mismatch of parameters in circuit 1. ΔV_P, ΔC_P, and ΔR_L are the mismatches of pinch-off voltage T1 and T2, two coupling capacitors C_P and load resistors R_L, respectively. ΔC_F is the relative tolerance of the feedback capacitor C_F, and $\Delta(R_F/R_{G2})$ is the tolerance of the ratio of the resistance R_F to R_{G2}. Two circuits are simulated, one is optimized at 1.67 GHz and the other one is optimized at 5.8 GHz.

From Table I, it is seen that the circuit has an excellent process tolerance, in the worst case the gain balance is only shifted by ± 0.4 dB at 5.8 GHz, and the phase balance is shifted by $\pm 1^\circ$. Fig. 6 is the measured performance of circuit 1 against variation of V_{DD}. Compared with the results published in [2]–[5], this circuit demonstrates much better performance.

The choice of the model used in the circuit will affect the accuracy of the circuit. Compared with results which use S-parameter dataset in the design, the performance of the phase splitter which uses EEFET3 model is obviously poorer, see Fig. 7. In the design that uses EEFET3 as the model, the gain difference of 1 dB and phase difference of 184° is observed, while in the design that uses S-parameter dataset, the gain difference is less than 0.5 dB, the phase difference is 181°, and it has a wider band performance than the previous one. This indicates how the accuracy is affected by choosing different MESFET models.

For circuit 2, Fig. 8 shows measured gain and phase differences versus frequency when tuning V_B externally. At 1.67 GHz (optimized operating frequency), by tuning external dc voltage V_B, the gain difference can vary from -3 to $+2$ dB while the change of the phase difference is within 3°. With circuit 2, the R_F mismatch or offset (not dc offset) of the differential amplifier next to circuit 2 can be cancelled by this external tuning. Therefore, circuit 2 provides a critical unbalance cancellation technique that can be used in high-performance RFIC's.

Both circuits consume 3.8-mA dc current. Their chip photos are shown in Fig. 9. Obviously, the feedback circuits do not consume any extra dc current. They are easy to understand and design.

IV. Conclusions

Two novel active differential phase splitters with *LCR* series feedback circuits have been proposed, designed, measured, and discussed. The feedback circuits can adjust gain and phase unbalance separately and accurately, without consuming extra dc current. The new circuits have excellent performance against process variations due to their inherent symmetrical topology. The circuits can achieve ± 1 dB and $180 \pm 1^\circ$ differential signals within 4-GHz bandwidth, well covering the frequencies for dual-band wireless communication. With the tunable feedback circuit, more accurately balanced differential signals can be achieved by external tuning. An accurate model for the transistor is essential in simulation for achieving accurate results. These circuit topologies can be extended to other technologies like CMOS, BiCMOS, or bipolar for RF applications. Compared with other active baluns, the new circuits feature simplicity, low power supply, wide-band performance, and consume small die area at lower microwave frequencies.

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Huainan Ma (M'93) received the bachelor's, master's, and Ph.D. degrees in electronics engineering from Tsinghua University, Beijing, China, in 1983, 1986, and 1990, respectively.

From 1983 to 1986, he worked with the Institute of Microelectronics of Tsinghua University as a Research Assistant in development of the CMOS process. From 1987 to 1989, he worked with the CSEM (Centre Suisse D'Electronique et de Microtechnique S.A.), at Neuchatel, Switzerland, as a Research Assistant in development of ac and dc modeling of bipolar transistors compatible with CMOS technology. In 1990, he joined the Institute of Microelectronics of Tsinghua University as a Research Associate in the VLSI department, responsible for testing and design for testability of CMOS VLSI circuits. In 1992, he joined the IME (Institute of Microelectronics, Singapore) as a Member of the Technical Staff in the Department of VLSI Circuit Design and Test, where he did various projects on CMOS mixed-signal IC design and testing. He started RFIC activities of IME as the Project Leader. The projects included development of MMIC GaAs chip-set and single-chip RF transceivers for 1.9-GHz PHS application; 2.5- and 5.8-GHz MMIC design using TriQuint's TQTRX process. He has now joined the Wireless IC Design Center, Fujitsu Microelectronics, Dallas, TX, as a Leading Engineer, starting CMOS RFIC. His current research interests are in the design of front-end RFIC for wireless applications and RFIC design methodology.

Dr. Ma was the recipient of the Outstanding Master Thesis and Outstanding Ph.D. Dissertation of Tsinghua University.

Sher Jiun Fang received the B.Sc. degree from the State University of New York at Buffalo in 1991 and the M.Eng. degree from the National University of Singapore in 1996.

From 1991 to 1992, she was with the TriTech Microelectronics, Singapore, where she was involved in the design of frequency synthesizers. In 1992, she joined the Institute of Microelectronics, Singapore, where she developed continuous-time filters and mixed-signal IC's between 1992 and 1995. Since 1996, she has been engaged in the upconverter design of the PHS system and responsible for the design methodology and CAD setup of the RFIC design environment. Her current research interests are in the area of CMOS RFIC for wireless communications.

Ms. Fang is a member of the Golden Key National Honor Society, Tau Beta Pi, and Eta Kappa Nu.

Fujiang Lin (M'93) received the B.S.E.E. and M.S.E.E. degrees from the University of Science and Technology of China (USTC), Hefei, China, in 1982 and 1984, respectively, and the Dr.-Ing. degree from the Universitit Kassel, Germany, in 1993, all in microwave and RF engineering.

From 1984 to 1986, he served as a Teaching and Research Assistant at the USTC in the areas of electromagnetic field theory and microwave antennas. From 1987 to 1989, he worked as a Research Engineer at the Technische Universität Hamburg-Harburg, Germany, where he was involved with the theoretical investigation of microwave oven optimization and CAD for millimeter wave coupled cavity traveling wave tubes. From 1989 to 1993, he was a Research Engineer at the Universität Kassel, Germany, where he focused on experimental modeling of high-performance microwave GaAs FET's. From 1993 to 1995, he was a Research Scientist at the National University of Singapore, where his research activities include microwave measurement techniques, large-signal FET modeling, and hybrid MIC's. Since 1995, he has been working with the Institute of Microelectronics (IME), Singapore, as a Member of Technical Staff. His area of focus is the modeling of RF devices and packages for the development of MMIC's. He is the Project Leader of RF modeling. Currently his interests extend to RFIC design onto MCM platform and he is the leader of this core project.

Hiroshi Nakamura was born in Fukuoka, Japan, in 1954. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from Tokyo University, Japan, in 1977, 1979, and 1982, respectively.

He joined the Oki Electric Industry Co., Ltd., in 1982. From 1982 to 1986, he was engaged in the R&D of GaAs digital IC processes. From 1986 to 1996, he was in the development of GaAs microwave IC design especially for the wireless applications. Since October 1996, he has been working for Oki Techno Centre (Singapore) Pte. Ltd., conducting several RFIC development projects for wireless communications.

Dr. Nakamura is a member of IEICE of Japan.